WHAT IS CLAIMED IS:

1. A method of inspecting a semiconductor wafer comprising the steps of:

(a) carrying out an inspection including a predetermined inspection object item for a semiconductor wafer, thereby obtaining inspection information by which a position on said semiconductor wafer of a nonstandard portion satisfying no inspection standard can be recognized;

(b) virtually dividing a virtual wafer corresponding to said semiconductor wafer under a predetermined dividing condition, thereby generating a virtual divided wafer having a plurality of virtual dividing unit cells arranged virtually;

(c) checking said inspection information over said virtual divided wafer, thereby obtaining the number of standard cells which do not include said nonstandard portion in said virtual dividing unit cells; and

(d) calculating a usable cell rate to be a ratio of said number of said standard cells to the total number of said virtual dividing unit cells.

2. The method of inspecting a semiconductor wafer according to claim 1, wherein

said predetermined inspection object item includes plural kinds of inspection object items, and

said inspection information includes information of each of said plural kinds of inspection object items by which a position on said semiconductor wafer of said nonstandard portion can be recognized.

3. The method of inspecting a semiconductor wafer according to claim 1, wherein

said predetermined dividing condition includes plural kinds of dividing conditions,

said virtual divided wafer includes plural kinds of virtual divided wafers which are virtually divided under said plural kinds of dividing conditions,

said step (c) includes the step of checking said inspection information over each of said plural kinds of virtual divided wafers, thereby obtaining the number of said standard cells in each of said virtual divided wafers,

said step (d) includes the step of calculating said usable cell rate in each of said virtual divided wafers, and

the method of inspecting a semiconductor wafer further comprises the step of:

(e) synthetically deciding quality of said semiconductor wafer based on said usable cell rate in each of said virtual divided wafers.

4. The method of inspecting a semiconductor wafer according to claim 1, wherein

said semiconductor wafer includes an SOI wafer to be a wafer having an SOI structure, and

said predetermined inspection object item includes a thickness of an SOI layer of said SOI wafer.

5. The method of inspecting a semiconductor wafer according to claim 1, wherein

said semiconductor wafer includes an SOI wafer to be a wafer having an SOI

structure, and

said predetermined inspection object item includes a thickness of a buried insulating layer of said SOI wafer.

6. The method of inspecting a semiconductor wafer according to claim 1, wherein

said semiconductor wafer includes an SOI wafer to be a wafer having an SOI structure, and

said predetermined inspection object item includes a loss of an SOI layer of said SOI wafer or losses of said SOI layer and a buried insulating layer.

7. The method of inspecting a semiconductor wafer according to claim 1, wherein

said semiconductor wafer includes an epitaxial wafer, and

said predetermined inspection object item includes a hillock-shaped defect of said epitaxial wafer.

8. The method of inspecting a semiconductor wafer according to claim 1, wherein

said predetermined inspection object item includes a COP (Crystal Originated Particle).

9. The method of inspecting a semiconductor wafer according to claim 1, wherein

said predetermined dividing condition includes a condition based on a shape

and size of a real device to be actually formed on said semiconductor wafer.

10. The method of inspecting a semiconductor wafer according to claim 1, wherein

said virtual wafer includes first and second inspection object areas,

said virtual dividing unit cells include a plurality of first and second virtual dividing unit cells present in said first and second inspection object areas respectively,

said inspection standard includes first and second inspection standards which are different from each other,

said nonstandard portion includes first and second nonstandard portions,

said standard cell includes first and second standard cells,

said inspection information includes information capable of recognizing said first nonstandard portion which does not satisfy said first inspection standard for said first inspection object area and said second nonstandard portion which does not satisfy said second inspection standard for said second inspection object area, and

said step (c) includes the step of calculating the numbers of said first standard cells which do not include said first nonstandard portions in said first virtual dividing unit cells, and the number of said second standard cells which do not include said second nonstandard portions in said second virtual dividing unit cells.

11. The method of inspecting a semiconductor wafer according to claim 10, wherein

said first inspection object area includes a memory cell area, and

said second inspection object area includes a peripheral area.

12. The method of inspecting a semiconductor wafer according to claim 1, further comprising the step of:

(f) deciding a value of said semiconductor wafer based on said usable cell rate obtained at said step (d).